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Special Section on

Computational Techniques for Advanced Packaging and Heterogeneous Integration

Expected online publication: 2025 Volume

The 2025 volume of the IEEE Journal on Multiscale and Multiphysics Computational Techniques (IEEE J-MMCT) will include a special section dedicated to 'Computational Techniques for Advanced Packaging and Heterogeneous Integration'. With the sustained miniaturization of device and circuit feature sizes coupled with the increasing functionality of integrated circuits, packaging has emerged as a critical area of focus in the chip-package-system ecosystem. To reduce interconnect lengths and the associated signal and power integrity issues that come with long line lengths, various design strategies are being explored in modern packaging. Moreover, with the growth of diverse technologies (e.g., wearable devices, IoT, newer 2D materials, advanced sensors, chiplets, and photonics), there is a push for heterogeneous integration of manufactured components into higher level assembly via advanced packaging techniques. This increased focus on advanced packaging requires the development of computationally efficient modeling and simulation tools for detailed verification, optimization, and virtual prototyping in the pre-fabrication stage. These tools must be able to model the electromagnetic compatibility, thermal, mechanical, and circuit performance of packaging structures for a thorough exploration of the reliability and cost-effectiveness of such packaging solutions. In this special section of the IEEE Journal of Multiscale and Multiphysics Computational Techniques, the focus will be on the development of the mathematical and computational theories, algorithms, and strategies that will be the core of such tools.

In this special section, we invite original papers describing novel computational methods and techniques for modeling and signal/power integrity verification of advanced packaging structures. These papers must be expanded versions of those accepted in the 17th IEEE Electrical Design of Advanced Packaging and Systems symposium organized in Bengaluru, India in December 2024. Areas of interests include, but are not limited to:

- 3D-ICs/TSVs/Interposers
- Signal and Thermal Integrity Verification and Analysis
- Computational Electromagnetics and Multi-physics Modeling
- Thermal Management Design for 3D-ICs and SiP
- Design and Modeling for High-speed Channels and Interconnects
- High-Speed Serial Links Jitter Budgeting
- Jitter Analysis and Modeling Algorithms and Tools
- Nanoelectronics for 3D-ICs and SiP
- Machine Learning Applied to Packaging
- Active Devices and Circuit Modeling Technologies

The J-MMCT Editorial Board will review every paper in the same manner as any other regular submission.
Paper submission is accomplished through the IEEE author portal link:

https://ieee.atyponrex.com/submission/dashboard

When you prepare your manuscript you should consult the instructions, templates, and resources available at the IEEE Authors' Center (https://ieeeauthorcenter.ieee.org). Papers not following the standard IEEE journal template cannot be accepted into the peer review process. Please be aware that your contribution should be **prepared as any other regular J-MMCT paper** and that it will be evaluated via the same peer-review process. The quality of your contribution **must meet the level required for a publication at J-MMCT**.

Other Submission instructions:

You must reference your own work, especially recent journal/conference publications including your EDAPS 2024 paper. Discuss your related publications in the introduction. Distinguish the new results you present in your current manuscript from those found in your EDAPS paper, **to demonstrate that the paper includes sufficient new technical material to justify a new paper, when compared to all previously published papers**.

Submissions are accepted any time, but no later than **May 14, 2025**.

If you have any questions, you can contact the Editor-in-Chief (Prof. Costas Sarris at eic-jmmct@ieee.org), or the Guest Editors:

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